Appln. No. 10/070,013
Supplemental Amdt. dated June 8, 2005
Reply to Office Action of August 25, 2004

PATENT

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A radio frequency (RF) up-convertor with reduced local oscillator leakage, for ~~modulating~~ emulating the modulation of an input signal $x(t)$ with a local oscillator signal having frequency f, said up-convertor comprising:

a synthesizer for generating mixing signals φ_1 and φ_2 which vary irregularly over time, where:

$\varphi_1 * \varphi_2$ has significant power at the frequency f of a said local oscillator signal being emulated~~, and~~;

neither φ_1 nor φ_2 has significant power at the frequency f of said local oscillator signal being emulated, and~~;~~

said mixing signals φ_1 and φ_2 are designed to emulate said local oscillator signal having frequency f in a time domain analysis;

a first mixer coupled to said synthesizer for mixing said input signal $x(t)$ with said mixing signal φ_1 to generate an output signal $x(t)\ \varphi_1$; and

a second mixer coupled to said synthesizer and to the output of said first mixer for mixing said signal $x(t)\ \varphi_1$ with said mixing signal φ_2 to generate an output signal $x(t)\ \varphi_1\ \varphi_2$, said output signal $x(t)\ \varphi_1\ \varphi_2$ emulating the modulation of said input signal $x(t)$ with said local oscillator signal having frequency f.

2. (Previously presented) The radio frequency (RF) up-convertor of claim 1 wherein said synthesizer further comprises:

a synthesizer for generating mixing signals φ_1 and φ_2, where $\varphi_1 * \varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)\ \varphi_1\ \varphi_2$.

3. (Currently amended) The radio frequency (RF) up-convertor of claim ~~2~~ 1 wherein said synthesizer further comprises:

a synthesizer for generating mixing signals φ_1 and φ_2, where $\varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)$ φ_1 φ_2.

4. (Original) The convertor of claim 3, further comprising:

a closed loop error correction circuit.

5. (Previously presented) The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit for measuring an error in said output signal $x(t)$ φ_1 φ_2; and

a time-varying signal modification circuit for modifying a parameter of one of said mixing signals φ_1 φ_2 to minimize said error level.

6. (Original) The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a power measurement.

7. (Original) The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a voltage measurement.

8. (Original) The radio frequency (RF) up-convertor of claim 5, wherein said error level measurement circuit comprises a current measurement.

9. (Previously presented) The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter is the phase delay of one of said mixing signals φ_1 and φ_2.

10. (Previously presented) The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter is the fall or rise time of one of said mixing signals φ_1 and φ_2.

11. (Previously presented) The radio frequency (RF) up-convertor of claim 5, wherein said modified parameter includes both the phase delay and the fall or rise time of one of said mixing signals φ_1 and φ_2.

12. (Previously presented) The radio frequency (RF) up-convertor of claim 3 wherein said synthesizer further comprises:

a synthesizer for generating mixing signals φ_1 and φ_2, where said mixing signals φ_1 and φ_2 can change with time in order to reduce errors.

13. (Original) The radio frequency (RF) up-convertor of claim 3, further comprising:

a DC offset correction circuit.

14. (Original) The radio frequency (RF) up-convertor of claim 13, wherein said DC offset correction circuit comprises:

a DC offset generating circuit for generating a DC offset voltage;

a summer for adding said DC offset voltage to an output of one of said mixers; and

a DC error level measurement circuit for modifying the level of said DC offset voltage to minimize error level.

15. (Original) The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a power measurement circuit.

16. (Original) The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a voltage measurement circuit.

17. (Original) The radio frequency (RF) up-convertor of claim 14, wherein said DC error level measurement circuit comprises a current measurement circuit.

18. (Original) The radio frequency (RF) up-convertor of claim 1, further comprising: a filter for removing unwanted signal components.

19. (Original) The radio frequency (RF) up-convertor of claim 18, where said filter comprises:

a filter for removing unwanted signal components from said $x(t)$ φ_1 signal.

20. (Currently amended) The radio frequency (RF) up-convertor of claim 1, wherein said mixing signal~~s φ_1 and~~ φ_2 ~~are random~~ is a square wave.

21. (Currently amended) The radio frequency (RF) up-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 ~~are pseudo-random~~ effect the modulation of an in-phase component of said input signal $x(t)$, and a complementary up-convertor with mixing signals 90 degrees out of phase, is used to effect the modulation of a quadrature component of said input signal $x(t)$.

22. (Previously presented) The radio frequency (RF) up-convertor of claim 1, wherein said synthesizer uses a single time base to generate both mixing signals φ_1 and φ_2.

23. (Previously presented) The radio frequency (RF) up-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are digital waveforms.

24. (Previously presented) The radio frequency (RF) up-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are square waveforms.

25. (Original) The radio frequency (RF) up-convertor of claim 3, further comprising:

a local oscillator coupled to said synthesizer for providing a periodic signal having a frequency that is an integral multiple of the frequency of said local oscillator signal being emulated.

26. (Original) The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit comprises a digital signal processor (DSP).

27. (Original) The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit comprises analogue components.

28. (Previously presented) The radio frequency (RF) up-convertor of claim 4, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit for measuring an error in said output signal $x(t)$ φ_1; and

a time-varying signal modification circuit for modifying a parameter of one of said mixing signals φ_1 and φ_2 to minimize said error level.

29. (Previously presented) The radio frequency (RF) up-convertor of claim 1, where said synthesizer uses different patterns to generate signals φ_1 and φ_2.

30. Canceled.

31. (Currently amended) A method of modulating a baseband signal $x(t)$ comprising the steps of:

generating mixing signals φ_1 and φ_2 which vary irregularly over time, where:

$\varphi_1 * \varphi_2$ has significant power at the frequency f of a local oscillator signal being emulated~~, and~~;

neither φ_1 nor φ_2 has significant power at the frequency f of said local oscillator signal being emulated~~;~~, and

said mixing signals φ_1 and φ_2 are designed to emulate said local oscillator signal having frequency f, in a time domain analysis;

mixing said input signal $x(t)$ with said mixing signal φ_1 to generate an output signal $x(t)$ φ_1; and

mixing said signal $x(t)\ \varphi_1$ with said mixing signal φ_2 to generate an output signal $x(t)\ \varphi_1\ \varphi_2$.

32. (Currently amended) An integrated circuit comprising the radio frequency (RF) up-convertor of ~~any one of claims 1 – 29~~ claim 1.

33-34. Canceled.